

**EAST - [10699839.wsp:1]**

File View Edit Tools Window Help

☐ Drafts  
☐ Pending  
☒ Active  
☐ Failed  
☐ Saved  
☐ Favorites  
☐ Tagged (0)  
☐ UDC  
☐ Queue  
☐ Trash

L1: (1) ("5959308").PN.  
 L2: (1) ("5879962").PN.  
 L3: (1) ("5473174").PN.  
 L4: (1) ("5308444").PN.  
 L5: (1) ("5438951").PN.  
 L6: (1) ("5238869").PN.  
 L7: (1) ("5183776").PN.  
 L8: (1) ("5141893").PN.  
 L9: (1) ("6291321").PN.  
 L10: (1) ("6107635").PN.  
 L11: (0) ("GaAs and SiGe and (Ge germanium) and annealing").PN.  
 L12: (778) GaAs and (silicon Si) and SiGe and annealing and (Ge germanium)  
 L13: (8) GaAs and (silicon Si) and SiGe and high temperature near annealing and (Ge germanium)  
 L14: (341) GaAs and (silicon Si) and SiGe and annealing and (Ge germanium) and ("70" wt% 70%)  
 L15: (19) GaAs and (silicon Si) and SiGe and annealing and (Ge germanium) and ("70" wt% 70%) wt

Search:       
 DB: US-PG-PUB, US-PAT, EPO ☐ Europe  
 Default operator: OR ☐ Highlight all found items only

GaAs and (silicon Si) and SiGe and annealing and (Ge germanium) and ("70" wt% 70%) wt Ge

4

	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	<input type="checkbox"/>	<input type="checkbox"/>	US 20050023552 A1	20050203	8	Growth of GaAs epitaxial layers on Si substrate by using a novel GeSi buffer layer	257/103	
2	<input type="checkbox"/>	<input type="checkbox"/>	US 20040256613 A1	20041223	35	Semiconductor device, semiconductor circuit module and manufacturing method of the same	257/19	257/E21.066; 257/E21.633; 257/E21.064
3	<input type="checkbox"/>	<input type="checkbox"/>	US 20040157412 A1	20040812	12	Method to produce germanium layers	438/478	257/E21.129; 257/E21.131; 438/489
4	<input type="checkbox"/>	<input type="checkbox"/>	US 20040137685 A1	20040715	19	Gate material for semiconductor device fabrication	438/285	257/E21.202; 257/E21.203; 257/E21.434
5	<input type="checkbox"/>	<input type="checkbox"/>	US 20040115916 A1	20040617	28	Selective placement of dislocation arrays	438/597	
6	<input type="checkbox"/>	<input type="checkbox"/>	US 20040092051 A1	20040513	12	Methods for preserving strained semiconductor substrate layers during CMOS processing	438/22	257/18; 257/19
7	<input type="checkbox"/>	<input type="checkbox"/>	US 20040072409 A1	20040415	17	Coplanar integration of lattice-mismatched semiconductor with silicon via wafer bonding virtual substrates	438/455	257/E21.568; 257/E21.569; 438/458
8	<input type="checkbox"/>	<input type="checkbox"/>	US 20040031979 A1	20040219	64	Strained semiconductor-on-insulator device structures	257/233	257/235; 257/297; 257/E21.415
9	<input type="checkbox"/>	<input type="checkbox"/>	US 20040005740 A1	20040108	35	Strained semiconductor-on-insulator device structures	438/149	257/347; 257/349; 257/352
10	<input type="checkbox"/>	<input type="checkbox"/>	US 20030227057 A1	20031211	21	Strained semiconductor-on-insulator device structures	257/347	257/E21.415; 257/E21.442; 257/E21.448
11	<input type="checkbox"/>	<input type="checkbox"/>	US 20020106882 A1	20020808	7	Method of producing a semiconductor layer on a substrate	438/605	257/E21.57; 438/201

rt

BEST AVAILABLE COPY